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What we claim is:

1	1. A process for forming at least one transistor on a substrate,
2	which process comprises depositing on the substrate at least one layer of
3	semiconductor material, wherein the substrate comprises a polyphenylene polyimide.
1	2. A process according to claim 1 wherein the polyphenylene
2	polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.
1	3. A process according to claim 2 wherein the polyimide is a
2	derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine.
1	4. A process according to claim 1 wherein a passivating layer is
2	deposited on the substrate before the semiconductor material is deposited thereon.
1	5. A process according to claim 4 wherein the passivating layer
2	comprises silicon dioxide or aluminum nitride.
1	6. A process according to claim 4 wherein the passivating layer
2	has a thickness in the range of about 20 to about 100 nm.
1	7. A process according to claim 4 wherein the passivating layer is
2	deposited on both surfaces of the substrate.
1	8. A process according to claim 4 wherein the substrate is heated
2	to a temperature greater than about 150°C for a period of at least about 1 minute
3	before deposition of the passivating layer.
1	9. A process according to claim 4 wherein the substrate is heated
2	to a temperature greater than about 250°C for a period of at least about 5 hours after
3	deposition of the passivating layer.
1	10. A process according to claim 1 wherein the substrate is heated
2	to a temperature greater than about 250°C for a period of at least about 1 hour before
3	deposition of the semiconductor material.
1	11. A process according to claim 1 wherein the substrate comprises

a metal layer on the side thereof remote from the semiconductor material.

1	12. A proc	ess according to claim 11 wherein the metal layer has	
2	walls defining apertures extending through the metal layer.		
1	13. A proc	ess according to claim 1 wherein the deposition of the	
2	semiconductor material is effected at a temperature in excess of about 300°C.		
1	14. A pro-	cess according to claim 1 wherein a metal layer is	
2	deposited upon the substrate on the same side thereof as the semiconductor materia		
3	but prior to the deposition of the semiconductor material.		

- 15. A process according to claim 14 wherein the metal layer comprises chromium.
- 16. A process according to claim 14 wherein the metal layer is deposited as a continuous film and is thereafter patterned prior to deposition of the semiconductor material thereon.
- 17. A process according to claim 14 wherein a layer of dielectric material is deposited over the metal layer prior to the deposition of the semiconductor material.
- 18. A process according to claim 17 wherein the dielectric layer comprises silicon nitride.
- 19. A process according to claim 1 wherein the dielectric layer is deposited by plasma enhanced chemical vapor deposition.
- 20. A process according to claim 1 wherein the semiconductor material comprises amorphous silicon.
- 21. A process according to claim 20 wherein the semiconductor material is deposited by plasma enhanced chemical vapor deposition.
- 22. A process according to claim 20 wherein the amorphous silicon is not patterned so that it extends continuously between at least some pairs of adjacent transistors

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1	23.	A process according to claim 20 wherein the semiconductor	
2	material further comprises a layer of n-type silicon deposited over the amorphous		
3	silicon.		
1	24.	A process according to claim 23 wherein a continuous layer of	
2	the n-type silicon is deposited over the amorphous silicon, a patterned layer of metal is		
3	thereafter formed over the n-type silicon, and the resultant structure is thereafter		
4	etched to remove portions of the n-type silicon not covered by the patterned layer of		
5	metal.		
1	25.	A process according to claim 1 wherein deposition of the	
2	semiconductor material is effected on a continuous web of substrate.		
1	- 26.	A substrate comprising a polyphenylene polyimide, the	
2	substrate bearing at least one transistor		
1	27.	A substrate according to claim 26 wherein the polyphenylene	
2	polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.		
1	28.	A substrate according to claim 27 wherein the polyimide is a	
2	derivative of biphenyl-3,3',4,4'-tetracarboxytic acid and an α,ω-alkanediamine.		
1	29.	A substrate according to claim 26 having a passivating layer	
2	between the substrate	e and the transistor.	
1	30.	A substrate according to claim 27 having a metal layer on the	
2	side thereof remote from the transistor.		
1	31.	A substrate according to claim 27 wherein the transistor	
2	comprises at least one amorphous silicon layer.		
1	32.	A substrate according to claim 31 bearing at least at least two	
2	transistors, each of the transistors comprising at least one amorphous silicon layer and		
3	the silicon layer extending continuously between the two transistors.		
1	33.	A substrate according to claim 27 wherein the transistor further	

comprises at least one n_ptype silicon layer in contact with the amorphous silicon layer.